Development of an LFSR Based Test Pattern Generator for Functional Logic Testing

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Abstract
This paper presents the development of an LFSR based test pattern generator (TPG) to test the functional logic of combinational and sequential circuits. Primitive polynomial based LFSRs and deterministic testing algorithms are applied simultaneously on the circuit under test (CUT) to detect the fault with minimum test length. Fault simulation was performed on ISCAS'85 and ISCAS'89 benchmark circuits using digital fault simulators FSIM and Tetramax. The proposed technique achieved complete fault coverage with shorter test sequences and required less hardware for its implementation.

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About the Speaker

Zahid received his BEng with First Class from Khulna University of Engineering and Technology (KUET), Bangladesh in 2000. He started his Master of Science at Universiti Kebangsaan Malaysia after his undergraduate study in 2001. For his research progress the authority allow him to lead as PhD candidate in 2003. Currently he submitted his PhD thesis. Zahid’s research interest is in the area of VLSI circuit testing and Biomedical Instrumentation.